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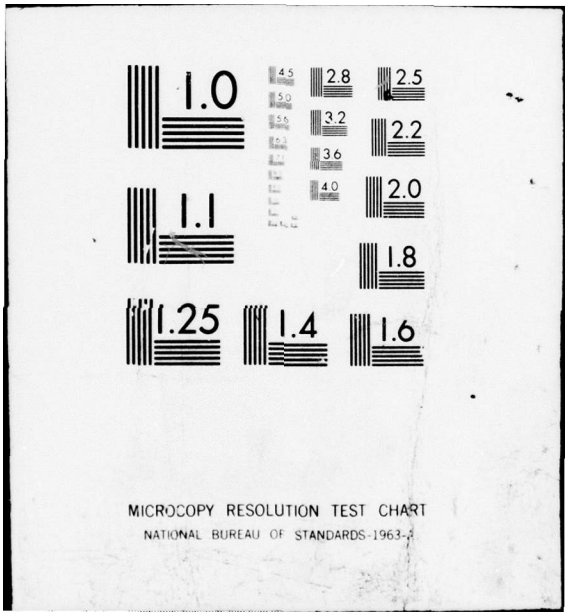
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STANFORD ELECTRONICS LABORATORIES

DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

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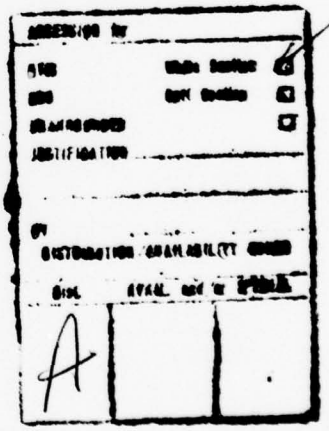

J. D. Meindl, Director
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CONTENTS

ILLUSTRATIONS

I. RESEARCH PROGRAM

A. Real-Time Statistical Data Processing and Fast-Estimation Algorithms

Principal Investigators: T. Kailath, M. Morf

1. Objectives

We have become aware that our fast algorithms have roots in and connections to certain physical wave-propagation and scattering phenomena. We are pursuing these connections slowly by attempting to place the fairly vast physics and mathematics literature relating to this topic in a more engineering and signal-estimation-oriented framework. To this end, we have been working with Professor Harry Dym of Israel who is co-author of the most recent comprehensive but quite abstract book on the inverse-scattering problem. Preliminary results indicate that we can adapt the well-tested estimation algorithms of modern control and communication theory to find new computationally efficient solutions to the inverse-scattering problem. These investigations are making contact with some of our earlier work on reproducing kernel Hilbert spaces and operator factorization, and this has led to the strong possibility that one of the best-known mathematicians in this field, Professor A. Schumitzky of USC, will spend half of his sabbatical leave at Stanford University (July 1979 to February 1980).

2. Current Status of Work

We have been involved in a wide range of activities in the general field of statistical signal processing. Our work during the past year is summarized below.

a. Signal Estimation for State-Space Models

The so-called "square root" methods are beginning to emerge as perhaps the most numerically stable algorithms for estimation in state-space systems, especially in trajectory analysis, navigation, and guidance. Important problems are error and sensitivity analysis.

Based on a geometrical interpretation of square-root filtering,[†] we have developed square-root arrays for assessing the effect of changes in the model parameters.

We have studied algorithms for continuous-time systems and have realized a new analog implementation that avoids an arbitrary triangular matrix operation required in earlier solutions to this problem.

We have demonstrated how square-root methods may be combined with parallel-processing schemes to speed up the computations in large-scale systems. A consequence of these results is a new square-root doubling formula for computing the solution of the algebraic Riccati equation encountered in stationary control and estimation theory. This new algorithm enables us to address a wider class of problems (with singular state-transition matrices) than previously known.

John Newkirk has made a connection between scattering-theory interpretations of least-squares estimation and square-root filtering. This connection has generated a simpler derivation and some computationally less complex versions of the square-root doubling algorithm. Newkirk's work also contains results of actual numerical comparisons between the new method and the currently available techniques for solving the ARE.

Several invited surveys of our results were presented at recent meetings.

b. Spectral Estimation

The "maximum entropy" (or "autoregressive fitting") method of spectral estimation has become popular among scientists when high-resolution estimates are required for short data samples. Several questions concerning the statistical properties of such estimators

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[†]Morf and Kailath, Automatic Control Transactions, Aug. 1975.

still remain unanswered; however, a number of people in several fields (at the Naval Undersea Labs in New London and at the National Oceanic and Atmospheric Agency in Boulder) and many geophysical (oil-exploration) companies have extended this technique to multichannel observations. By expanding the ideas encountered in our study of Toeplitz matrices, we have obtained what appears to be the best solution to this long-standing problem. An invited paper describing our solution is being reprinted[†] (as are others) in a forthcoming IEEE Press book on modern spectral analysis.

c. Two-Dimensional Systems

It has only been a few years since attempts have been made to extend the many results obtained from linear system theory for one-dimensional systems to 2-D systems that arise directly in image-processing; however, mathematical theory is also applicable to certain one-dimensional problems--especially systems with lumped and distributed elements or delay-differential systems. In the last two decades, state-space models have dominated the field of linear system theory but, in the early 1970s, a counter revolution developed in which transfer-function methods were renewed and were found to be very illuminating for one-dimensional systems.

We have also contributed to this field, but our major new success has been in extending them to 2-D systems wherein the transfer-function approach requires the functions of two complex variables and some algebraic geometry. Our findings have clarified and extended many results and conjectures in the state-space approach. For example, a central condition of one-dimensional system theory is that a realization is controllable and observable if and only if it is minimal. Similar results were anticipated in the 2-D case; however, the existing definitions led to examples of controllable and observable 2-D systems that

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[†]Morf, Leung, Lee, Kailath, "Recursive Multichannel Maximum Entropy Spectral Estimation," to appear in Modern Spectral Analysis, IEEE Press, 1979.

were not minimal and, conversely, of minimal 2-D systems that were not controllable and observable. The transfer-function approach also led to new definitions in which the equivalence between minimality and controllability and observability was restored. Other results have been published, and one has been selected for a forthcoming IEEE reprint book on multidimensional systems.[†]

3. Achievements

The most significant accomplishments of this research are as follows.

- A new "square-root doubling" method has been developed for solving the algebraic Riccati equation (ARE) widely encountered in optimal control and estimation theory. This new method has a substantially wider domain of application than currently available methods, and its numerical properties are not inferior to and are often substantially superior to the present methods.
- A long standing problem in geophysics (the so-called "maximum entropy" method for spectral analysis of multichannel data as obtained, for example, in oil exploration) has been solved.
- Algebraic geometry and methods are being used in the analysis of two-dimensional systems as arise, for example, in imaging problems and in studying differential equations.

[†]Morf, Lévy, Kung, "New Results on 2-D Systems Theory. Part I: 2-D Polynomial Matrices, Factorization, and Coprimeness," Proc. IEEE, 65, June 1977, pp. 861-872.

B. Signal Processing and Compression

Principal Investigator: M. E. Hellman

1. Objectives

We are investigating the fundamental limitations on the performance and efficiency of communication networks, including multiuser in addition to point-to-point systems. We are also developing improved methods of signal processing for such systems from the structures used to confirm the performance limitations. Particular attention will be focused on methods (such as trellis encoding) that require only low-complexity signal processing. Signal processing for data compression, signal-to-noise-ratio improvement, and privacy will also be studied.

This work is motivated by the fact that military and civilian communication networks are becoming increasingly digital. Digital communication has the advantages of rapidly decreasing component cost, relatively high noise and jamming immunity, amenability to error control, and cryptographic coding for increased reliability and security. Its one disadvantage is a wider bandwidth. A speech signal that occupies 3 kHz of bandwidth in analog form requires ten or more times this bandwidth if digitized in a straightforward manner. The goal of source coding (alias bandwidth or data compression) is to remove redundancy or unnecessary detail from the data, thereby reducing the data rate and bandwidth. For example, vocoded speech is in digital form and occupies no more bandwidth than the original analog waveform.

The theory and practice of source coding have had significantly less overlap than the theory and practice of channel coding, and one goal of our research is to develop theoretical models more closely related to current techniques. This has the dual advantages of making the theory more useful and of suggesting interesting new theoretical models.

We plan to continue our work on speech compression by improving the algorithms used to find codebooks for vector quantization. This will facilitate the production of higher rate codebooks and a study of the first- and second-order probabilistic behavior of speech. We will also

attempt to adapt the tree-coding techniques to new speech spectral-distortion measures and to implement structured (noncodebook) techniques for quantization.

A whole new area of information theory has been developed during the last several years with the introduction of privacy constraints on communications. Wyner led this trend with his "wiretap channel" which is a broadcast channel with one transmitter and two receivers; however, it has the novel constraint that the information flow is maximized to the first (legitimate) receiver and minimized to the second (wiretapping) receiver. If the wiretapper's channel is noisier than the main channel, Wyner demonstrated that it is possible to communicate reliably to the first receiver while conveying absolutely no information to the second. The wiretap channel has been suggested as a model for optical communication from an aircraft to a submarine because the "wiretapper" can detect a low signal from light scattered at the ocean surface. Communication with directional antennas and with the wiretapper in a sidelobe also is well modeled.

It is sometimes possible for the receiver to send a feedback signal to the transmitter to aid communication on the forward link from the transmitter to the receiver. In many situations, this feedback signal will be overheard by the wiretapper, which results in a wiretap channel with public feedback. We have been concerned with the theoretical limitations on this channel's communication and secrecy capabilities.

Our achievable rate-secrecy region for the wiretap channel with public feedback is known to be suboptimal because a special coding scheme (based on a compounding of uncertainty) produces a larger region for the independent binary erasure channel. We strongly believe that this compounding effect does not increase the capacity region for the independent binary symmetric channel, and we intend to investigate this effect from the following questions.

> How may it be generalized to improve the known region, and is it possible to supply a simple description of the improved region?

Is there a class of channels in which compounding is not effective, and can such a class be characterized? If so, is our current region actually the capacity region for this class, and can we establish a converse?

All earlier work has assumed an unlimited-capacity feedback link. We will investigate performance degradation when the capacity is limited, and this will lead to an investigation of the wiretap channel with generalized feedback where forward and feedback channels interfere. Insight obtained from this study will be of value when we investigate the two-way channel with eavesdropper.

The Slepian-Wolf data-compression result has proved extremely valuable in understanding multiuser communication problems. We plan to extend this classic result to large families of correlated sources. We will also investigate the complementary problem of the multiple-access channel with correlated sources.

2. Current Status of Work

One objective of our work is to develop new theoretical models for data compression, which are more closely related to current data-compression techniques. This will make the theory of greater practical value and will suggest interesting new theoretical models.

The fake-process approach to data compression is based on the observation that, in theory, when driven by a random binary sequence, a good source decoder must produce an output sequence whose statistical properties are characteristic of the source. The problem is to design decoder output "filters" having this property. The resultant systems are moderately complex and typically outperform traditional techniques (such as delta modulation, optimal memoryless quantization, and predictive quantization) by 1 to 2 dB. Although not large, this improvement is obtained at very little increase in system complexity.

We have completed the initial phase of our research on the fake-process approach to tree-coding data compression. This work has been documented in technical reports and has been published as a paper.

Traditionally optimal quantization design requires a complete probabilistic model for the source to be quantized and uses variational techniques to obtain the quantizer. This presents practical difficulties because such precise knowledge of the source is rarely known. We have developed an algorithm that takes a given distortion measure, a training sequence from the source, and an initial estimate for the quantizer and iteratively improves the quantizer to produce a locally optimal quantizer.

Roughly speaking, the algorithm determines the best quantizer partition for a given set of output levels by mapping the input symbol into the closest reproduction level. It then finds the most satisfactory collection of reproduction symbols for a fixed partition by minimizing the conditional distortion of the sample for each element of the partition.

We have demonstrated that, if the source is stationary and ergodic and if the distortion measure is a power of the error signal (such as a mean-square error), the algorithm always converges in a finite number of steps. At the limit, as the training sample becomes large, the resulting quantizer converges to the optimal Lloyd-Max quantizer for the true (but unknown) statistics. This algorithm also works for vector sources and complex vector-distortion measures. This research has been completed, and a paper has been submitted for publication.

The vector-quantization technique described above has been used in a training sequence of linear predictive coded (LPC) speech samples, based on several spectral-distortion measures proposed by the speech community as candidates for measuring subjective distortion. We obtained "codebooks" of from 1 to 8 bits per frame for the 12 reflection coefficients produced by each frame of the LPC analysis.

Preliminary tests using the 7- and 8-bit/frame codebooks yielded speech with no perceptible degradation from the original LPC speech. This result must be viewed as preliminary because the original LPC speech was of poor quality. We are in the process of obtaining better-quality training data. These results are so encouraging, however, that they are discussed in further detail in the section describing our most significant achievements.

The speech codebook described above was combined with the fake-process technique to design a waveform tree-coding data-compression system in the 5 to 8 kbps range. As noted by Gold,† this is an important area for research:

> "However, there still remains an important data-rate gap among speech processing algorithms. Systems such as LPC ... work effectively between 2.5 and 4 kbps, but are not robust systems. APC can be made to work effectively between 8 and 16 kbps maintaining robustness. ... The gap is between 4 and 8 kbps; at present there exists no method of gracefully encompassing this important region and increasing robustness by increasing data rate. In our judgment, this is an important area for research."

The resulting system had a lower rate and was less complex than other existing tree-coding systems and had comparable speech quality. It used eight decoding filters chosen from the low-rate codebooks and an encoder that performs eight parallel tree searches. It selects the best available path and sends side information to the decoder to specify which filter to use. This generates an adaption capability without requiring on-line LPC analysis.

Other work combined data compression and decision theory and was directed toward verifying certain intuitive concepts in decision theory. Data are normally collected to facilitate decision making; as such, transmitting only one decision is an extreme form of data compression. Frequently, a collection of measurements is available but, for reasons of complexity, only a k-element subset of the measurements can be used which causes a measurement-selection problem.

In previous work, we established that any optimal measurement-selection algorithm for the Bayesian classification problem, or for the linear-regression problem with vector-valued regressors, must be exhaustive. Further analysis revealed that any assignment of probability of error to measurement subsets is possible, subject only to a simple

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†Proc. of the IEEE, Dec 1977.

monotonicity constraint. It can be concluded, therefore, that any counterexample to intuition can be found through these constructive techniques.

For many years, it has been stated in the literature that "more information may be worse than no information," which was originated by Hughes for Bayes classifiers. We have confirmed that this statement is false and have prepared a paper that resolves the apparent paradox by showing that Hughes made incorrect comparisons of statistically incomparable models to arrive at his conclusion.

In another area, we have developed relationships between maximum-entropy probability distributions and conditional probability. From a data-compression standpoint, we have demonstrated that, given an empirical average of the first n variables, the conditional distribution of a random variable is as incompressible as possible.

In work on broadcast and wiretap channels, we have determined an achievable region for the two-output broadcast channel with public feedback and a degraded message set consisting of common, private, and secret submessages. These submessages must be reliably decoded by the first receiver who can use a public feedback link to the transmitter (the second receiver also sees what is communicated on the feedback link). The common submessage is decoded by the second receiver, and the secret submessage must remain totally unintelligible. This region is an extension of the nonfeedback region described by Korner and Marton for the broadcast channel with degraded messages. We have derived an achievable rate-secrecy region for the general wiretap channel with public feedback which is a special case of the above model when there is no common message.

We have also developed a message precoding procedure which is a generalization of the Carleial-Hellman prescrambling approach to the wiretap channel. Based on this procedure, we have observed that the simpler rate-secrecy description is sufficient for evaluation of the more complex rate-equivocation region which, in turn, is equivalent to the region of public and secret submessages.

We also developed a theory and techniques for compressing dictionaries and other data bases when occasional incorrect answers to queries concerning the data base can be tolerated, as in typographical error-checking programs. Trade-offs between the amount of storage required and the accuracy desired were obtained.

We have also created algorithms for constructing optimal prefix-condition codes over finite alphabets with symbols of equal costs. When the messages are equally likely, the resulting algorithm generates a useful representation of an optimal code in almost less time than it takes to write down the code.

3. Achievements

Low data-rate digitized speech models the vocal tract as a linear filter and sends a description of this filter and its driving function so that the speech can be reproduced at the receiver. The filter is usually specified in terms of its quantized and transmitted reflection coefficients. Quantization of each reflection coefficient by itself is not totally optimal because the statistics required for an optimal vector quantization have been lacking. As a result, we applied the self-learning vector-quantization technique described above and obtained an approximately 6:1 compression on the data representing the reflection coefficients with no perceptible degradation in speech quality. The corresponding data rate was on the order of 600 bps.

This work is significant not only because of the low data rate obtained, but because it successfully uses speech-distortion measures that had been thought too complex to be mathematically tractable.

C. Description Languages and Design Tools for General-Purpose Computer Architectures

Principal Investigators: M. J. Flynn, W. M. vanCleemput, J. Hennessy

1. Objectives

We are developing description languages and other design aids to describe and implement computer architectures. We are also attempting to establish a basis for understanding the computer-design process.

2. Current Status of Work

a. The SPRINT Printed-Circuit Design System (K. Stevens, T. Bennett, W. M. vanCleemput)

The objective of the SPRINT system is to facilitate the interactive computer-assisted design of printed-circuit boards. SPRINT allows for the manual placement of critical components and for the automatic placement of such components as 14- and 16-pin dual in-line packages. The interconnection routing module manually routes critical connections and automatically routes noncritical connections. The current system is limited to two layers; however, an extension to multilayer boards is planned.

The input to SPRINT is the Structural Description Language (SDL). SDL is also used as input to a logic simulator, a fault test-generation/simulation system, and an automatic logic-diagram generation system.

SPRINT is implemented in MORTRAN and FORTRAN IV on the IBM 370 at SLAC and makes use of the Tektronix 4013 terminal. The SDL compiler is implemented in SPITBOL (a SNOBOL dialect). The output is in the form of a plot from which the artwork must be generated manually. Work is in progress to produce artwork automatically by means of a photoplotter. A component assignment subsystem is being completed in addition to an artwork editor.

b. Computer-Aided Layout of Large-Scale Integrated Circuits (E. Slutz, W. Marti, W. M. vanCleemput)

Although several systems exist for the automated layout of LSI circuitry, none obtains a layout comparable to one designed manually. We are developing and implementing a system based on algorithmic approaches in which certain decisions are the responsibility of the designer. It is expected that this system (now in its initial implementation phase) will reduce design time considerably and at no expense of excessive silicon area. The data base and interactive graphics functions are completed. Further work will investigate algorithmic approaches to layout automation.

c. Interactive System for Design Capture (A. von Bechtolsheim, W. M. vanCleemput)

In the current design system, all input is in the form of SDL, the Structural Design Language. Because designers often prefer schematic diagrams for their tasks, a system has been implemented that will take as its input a schematic drawing from an interactive graphics terminal and will output an SDL description for further processing by the various design-automation programs. The current version is written in MAINSAIL for the PDP 10 system. A more portable version, written in PASCAL, is being completed.

d. Implementation of a Digital Design Language (W. Cory, W. M. vanCleemput)

A compiler and simulator system for the DDL language is being implemented through a compiler-compiler scheme. The system is being written in PASCAL, which should provide a reasonable degree of portability, and is now operational.

e. Automated Generation of Logic Diagrams (J. A. Smith, W. M. vanCleemput)

The automatic generation of logic diagrams, originally developed at the University of Waterloo, Canada, has been reimplemented

and made compatible with the SDL input language. This system is written in MORTRAN, a structured FORTRAN preprocessor.

f. Description and Simulation of Computer Architectures
(D. Hill, W. M. vanCleemput)

The problem of describing and simulating a computer system at various levels of abstraction is being investigated. Currently, no adequate tools exist for simulating a design at multiple levels of abstraction. The current study focuses on the potential use of SIMULA for the multilevel simulation of digital systems.

g. Formal Description of a Real-Time Programming Language
(J. L. Hennessy)

The formal definition of TOMAL (Task-Oriented Microprocessor-Applications Language) is a programming language intended for real-time systems running on small processors. This definition addresses all phases of the language. Because some modes of semantic definition appear to be particularly well-suited to certain aspects of a language, and not as suitable for others, the formal description employs several complementary modes of definition.

The primary definition is axiomatic in the notation of Hoare; it is employed to define most of the transformations of data and control states affected by statements of the language. Simple denotational (but not lattice-theoretic) semantics complement the axiomatic definition to define type-related features, such as the binding of names to types, data-type coercions, and the evaluation of expressions. Combined, the axiomatic and denotational semantics define all the features of the sequential language.

An operational definition defines real-time execution and extends the axiomatic definition to account for concurrent execution. TOMAL does not impose rigid syntactic constraints on the use of shared data by concurrently executing program components; instead, a set of semantics dependent on the results of program execution delineates the conditions under which the axiomatic definition of the language will

hold. A version of these semantic constraints, sufficient to guarantee conformity with the axiomatic definition, can be verified by an analysis of a TOMAL program at compilation. This version may enforce slightly more stringent constraints than are necessary; when they are not observed by a program, the axiomatic semantics may not be applicable and the operational semantics will provide the language definition.

3. Achievements

In the current design system, all input is in the form of the SDL (structural design language). Designers, however, often prefer schematic diagrams for their tasks. An interactive system for design capture (IDSPEC) has been developed that will take as its input a schematic drawing from an interactive graphics terminal and will output an SDL description ready for further processing by the various design-automation programs. The IDSPEC is intended as a replacement for the Stanford University Drawing System (SUDS) which was developed at the Stanford Artificial Intelligence Laboratory. The original version of the IDSPEC was implemented on the DEC PDP 10 system, using the MAINSAIL language. A portable version, written in PASCAL, has become available.

D. Computer-Aided Design of VLSI

Principal Investigators: W. M. vanCleemput, B. Kumar

1. Objectives

The purpose of this study is to explore innovative approaches to the problem of IC layout. A further aim is to improve the current state of the art of automated IC layout to produce adequate tools for designing very large scale (VLSI) integrated circuits. The more specific goals are to

- obtain an accurate formulation of the circuit-layout problem
- analyze algorithmic efficiency for "typical" large-scale layout problems
- develop and evaluate hierarchical approach to IC layout
- produce efficient simulation tools that will be useful in the design of VLSI-based systems

These research objectives will be accomplished according to the following time schedule.

Current Year: Develop and implement a hierarchical approach to VLSI design

Second Year: Evaluate hierarchical design as compared to classical LSI design methods

Devise more accurate mathematical models and formulations for the circuit-layout problem

Study the use of simulation as a design tool in the VLSI environment

Third Year: Integrate new mathematical models into a real VLSI design system for practical evaluation

Analyze the algorithmic efficiency of various VLSI design algorithms

Continue the study of simulation to support VLSI system design

2. Current Status of Work

Research is under way to develop a hierarchical design approach for VLSI systems. To verify this methodology and its effectiveness, an IC layout system is being implemented. An interactive system for hierarchical design specification is now operational. The database for the IC system has been designed, and access routines have been implemented. Work is in progress on new automated placement and routing algorithms suitable for hierarchical IC layout. In addition, an interactive layout editing system is being implemented. A compiler for DDL (a digital design language) is now operational.

3. Achievements

The major achievements of this research are summarized as follows.

- An operational compiler and simulator for DDL (a digital design language) are completed. This implementation was written in PASCAL and should be portable for widespread use.
- Routing and placement algorithms for VLSI systems were developed and partially implemented. The principal innovation here is the ability to cope with arbitrary rectangular shapes, which has never before been accomplished.
- The database and philosophy for a hierarchical IC design facility were defined and partially implemented. This can be considered as the nucleus of a VLSI design system which, in time, will serve as a real test bed for VLSI design.

E. Reliability in Distributed Database Systems

Principal Investigators: S. S. Owicki, J. L. Hennessy

1. Objectives

We are developing methods for achieving reliability in a multicomputer distributed database system where data are stored, possibly redundantly, in a number of separate locations. We plan to study several system architectures and to devise algorithms for maintaining consistent data and an acceptable level of service, even when confronted with user errors or machine failures.

Our approach will be to develop and analyze such techniques as data organizations, algorithms, and communication protocols. We do not plan to implement a particular system although some components probably will be implemented for testing. Techniques will be evaluated analytically and by simulation for efficiency and degree of reliability.

The three-year program will be paced as follows.

Current Year: Study existing and proposed database systems (both centralized and distributed)

Identify a general set of functional requirements and common trouble spots

Develop and analyze basic algorithms

Second Year: Continue developing algorithms, concentrating on synchronization and robustness

Begin simulation for performance evaluation

Third Year: Add techniques for recovering after erroneous data are discovered

Analyze performance of various algorithms, considering interaction between system components

Develop an overall system design

A related problem is the question of process and data distribution. Given a description of the configuration of a distributed system and the description of the process environment, how should the processes

be distributed to maximize efficiency? To answer this question, methods for describing the distributed system, logical software configuration, and logical communication between processes will be explored. Using such information, we will search for feasible distribution approaches and study algorithms for automatically selecting process distributions.

2. Current Status of Work

Work on this project is at an early stage. We have analyzed several algorithms for maintaining the consistency of data in distributed databases and have considered both reliability and performance.

3. Achievements

A basic problem in distributed database systems is maintaining the consistency of data items as they are updated by different users. One method often used is to "lock" all the data involved in a user's transaction; this prevents other users from accessing these data for the duration of the transaction. Locking may reduce the amount of parallel activity in a system and can lead to deadlock.

A necessary and sufficient condition for the concurrent processing of transactions, without violating consistency, has been obtained, and a maximally concurrent and deadlock-free synchronization scheme was developed based on this condition. The limitations of the more common locking mechanisms have been determined, and the necessity of two-phase locking for consistency was proved when locking is the only mechanism for synchronization. NP-completeness of the shortest time transaction-scheduling problem has been demonstrated.

These results are interesting as theoretical bounds for concurrent processing. Despite some overhead, implementation of the maximally concurrent transaction-processing algorithm may be justified because it is deadlock-free.

F. Very Large Scale Integration

Principal Investigators: R. F. W. Pease, J. D. Meindl, W. E. Spicer, R. W. Dutton, R. M. Swanson, J. D. Plummer, D. R. Helms, I. Lindau, R. A. Powell, K. C. Saraswat, R. D. Melen, J. W. Knutti, H. V. Allen

1. Objectives

Since the introduction of the first planar transistor in 1959, the electronics industry has experienced an integrated-circuit revolution. Basically, the advance of integrated-circuit technology can be attributed to increases in packing density through reduction of line width, larger chip area and wafer size, cleverness in circuit design, better materials and fabrication processes, and advances in our understanding of device physics.

The number of elements per chip or complexity of integrated circuits has approximately doubled every year since their introduction in 1960. We are now on the threshold of very large scale integration (VLSI). At the same time, chip reliability has increased by several orders of magnitude and cost has remained virtually constant; however, this revolutionary rate of advancement may taper off prematurely because of a lack of concentrated effort to extend the necessary scientific base. Consequently, this section describes a coherent endeavor to probe several basic areas of materials and device physics fundamental to the progress of VLSI of greater than 10^5 elements per monolithic chip. Acquisition of a high-resolution projection-alignment system is considered essential for the conduct of this VLSI project.

2. Current Status of Work

a. Materials Analysis Studies for VLSI

A full basic understanding of many materials processes essential for VLSI technology is still in its infancy. Details of the silicon-oxide growth mechanism, its relationship to fixed charge (Q_{ss}), and its dependency on such parameters as oxide thickness, doping of bulk

Si on which the oxide is grown, growth time, and conditions are not well known. A strong program is under way in the Solid-State and Integrated-Circuit Laboratories at Stanford University to increase our knowledge in this area. The materials-analysis program in the Solid-State Laboratory is focused on an investigation of Si-SiO_2 interface region to

- determine experimentally the details of the topology and chemistry of this interface in terms of the growth parameters
- correlate this information with parameters essential for MOS device design and operation (such as Q_{ss}) and the pile up or depletion of doping impurities at the interface (including correlations with electrically active and inactive impurities)

Auger-sputter profiling (ASP) techniques have been developed to a very high level of sophistication in the Solid-State Laboratory. Reproducibility in depth resolution on the order of one angstrom is achieved regularly after sputtering through oxides with a thickness of 1000 Å. It has also been observed that the width of the transition region between Si and SiO_2 is a function of such parameters as oxide-growth temperature and Si-doping levels. In the limited studies to date, a correlation has also been found between the temperature of growth, interface width, and fixed charge Q_{ss} at the interface.

In a related series of studies, phosphorous pile up at the interface after oxidation is being analyzed as a function of the bulk P doping level in the silicon wafer. It has been noted that

- a large fraction of P originally in the oxidized Si is piled up sharply at the Si-SiO_2 interface
- much of P at the interface is not electrically active
- the sharp P pile up appears to be slightly on the Si side of the interface
- the width of the transition region from Si to SiO_2 increases (for a given oxidation process) with the P doping level.

The implications of these results and others in this continuing study of the electrical performance and fundamentals of oxide growth will be fully investigated. In addition to the studies using ASP, others are being developed based on photoemission techniques, including those at the Stanford Synchrotron Radiation Project (SSRP).

The interface, for example, between SiO_2 and Al deposited in various ways has also been investigated. Reducting SiO_2 to depths of over 100 Å and intermixing of Al_2O_3 results in the reduction of Si. Such analyses will continue on this and other systems and, again, will form a significant background for the VLSI studies proposed here.

This review of the current work related to the $Si-SiO_2$ interface in the Solid-State Laboratory was presented to gain a perspective for our work planned for VLSI. To date, we have concentrated primarily on perfecting the ASP techniques and instrumentation.

The research proposed here should begin 1 October 1978 and, by then, we should have a very strong background in terms of well-developed and available techniques and background knowledge of LSI systems on which our VLSI investigations can be based. The planned major expansion of the SSRP will provide (in addition to increased photoemission capabilities) the opportunity for X-ray lithography starting during FY 79, which is another capability available for this work if its utilization appears to be fruitful.

Importance of Interface Width for VLSI Devices

Scaling in VLSI devices dictates that, as dimensions are reduced parallel to the surface, element thicknesses must also be reduced. In our studies using Auger sputter profiling on the $Si-SiO_2$ interface, we have observed that the metallurgical interface for thermal oxides is approximately 20 Å, and it can be up to 50 Å or more for CVD oxides. For the thin-gate oxides necessary for VLSI MOS devices, the interface region can be 10 percent of the total thickness which, in turn, may have a major impact on device electrical properties. Based on the results of our previous studies plus new experimental work, we will attempt to correlate interface morphology with thin-oxide electrical properties.

Using ASP, we have found that the formation of electrical contacts of such materials as Al on SiO_2 form an interface region consisting of Al_2O_3 and Si at least 50 Å thick. This probably can be reduced by coevaporation of Al and other elements; however, this phenomenon will become more important in the area of VLSI and should be better understood. Because this transition region is a significant percentage of the total oxide thickness for thin oxides, it will have a major effect on the electrical characteristics of the device. Studies of these types of interfaces will concentrate on comparing various contact materials (Al, poly Si, and others) to determine the morphology and chemistry of the contact/SiO_2 interface.

Another important difference in processing thin oxides is dopant redistribution. For thin oxides, especially in the region of approximately linear growth, dopant pile up or depletion effects is expected to be very different from the thicker oxide regime where approximate steady state has been reached in the parabolic growth region. Based on our experience with thick oxides, we will determine dopant profiles as a function of substrate doping for thin oxides.

Effects of Large Current Densities

As device sizes become smaller, two-dimensional effects will become more important. The ability to study these effects through Auger electron spectroscopy (AES) will be determined by the beam size required and the current density necessary to achieve an acceptable signal-to-noise ratio. Current state-of-the-art equipment is available with a spatial resolution of approximately 2000 Å which would be adequate to study $\sim 1\ \mu$ structures in the plane parallel to the surface. In contrast, AES has been directed toward a higher resolution perpendicular to the surface. The depth probed into the sample is set by the very short inelastic escape length of the Auger electrons ($\lesssim 20$ Å) which gives the technique its high surface sensitivity. Lateral spatial resolution, however, is essentially the size of the cross section of the exciting electron beam. To achieve submicron spatial resolution with AES for VLSI application, therefore, highly collimated electron beams

are required which leads to large excitation current densities. Using a 10 μ spot, in our Auger laboratory, currents of $\lesssim 1$ μA are employed to produce current densities of $\lesssim 1$ A/cm^2; with a 0.1 μ spot, this same current leads to densities of $\simeq 10{,}000$ A/cm^2. Signal-to-noise considerations for the widely used cylindrical mirror electron-energy analyzer (CMA) cause excitation currents of less than 10^{-9} A to be impractical because of the long time constants required. Even at nanoampere currents, however, current densities necessary for lateral examination in VLSI applications are expected to be large ($\simeq 10$ A/cm^2).

It has been known for many years that surface composition can be changed by an incident electron beam. The severity of these changes depends on such factors as chemical composition of the sample studied, kinetic energy and current density of the incident beam, and total electron dose. Of interest to VLSI technology is the fact that many oxides (both metal and semiconductor oxides) decompose under prolonged electron beam exposure--the most pronounced beam interaction effect is the electron-stimulated desorption (ESD) of oxygen from the oxide. For example, Johannessen, Spicer, and Strausser have reported[†] that appreciable decomposition of SiO_2 into "free" Si occurs at current densities above ~3 μA/cm^2 at 2 keV. Because these effects on Si and metals are not as severe, studies of electrical contacts and doping distribution in highly doped substrates should be possible without interference from these decomposition effects; however, this must be determined. An additional electron-beam effect can occur on highly insulating samples, and a high electric field may be established normal to the surface under electron bombardment. This could lead to the field-assisted migration of charged mobile dopants (such as Cl^+ in SiO_2) toward or away from the surface, thereby changing the chemical depth profile of the dopant.

To summarize, if meaningful data are to be obtained from the use of AES with extremely high spatial resolution, the extent to

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[†] J. Appl. Phys., 47, 1976, p. 3028.

which the technique actually perturbs the surface being studied must be known. As knowledge in this area increases, beam interactions can be better understood and/or minimized by a suitable choice of such primary beam parameters as energy and flux. As a result, we plan to direct this research program toward a better understanding of the effect of electron beams used in AES on surfaces of practical interest to the semiconductor industry (such as SiO_2, Al_2O_3). Information gained in this manner should be applicable not only to AES but to any surface analytical techniques employing an electron beam (1 to 10 keV) as an excitation source.

X-Ray Lithography Using Synchrotron Radiation

The lithographic techniques employed within production processes today are based primarily on photolithography. The resolution in the generated pattern is typically on the order of 10 μm. One of the limiting factors is the diffraction effects of the light in the mask and the divergence of the light beam. Even with the new projection system available, 1 to 2 μm resolutions will be the limit.

X-ray lithography appears to be a promising technique for pattern generation on the submicron level. The diffraction effects are negligible because of the shorter wavelength compared to visible light. In comparison to e-beam lithography which also promises a reduction to submicron levels, X-ray lithography may have more uniform exposures and less sensitivity to dust or other particles on the wafer.

It appears that one of the limiting factors in the development of X-ray lithography has been the lack of suitable X-ray sources. Conventional X-ray tubes are used, with characteristic radiation lines of $h\nu \gtrsim 1.5$ keV which is far from the optimal wavelength for the most suitable X-ray optics or for the available photoresist materials. Instead, the most preferable photon-energy region for X-ray lithography is 300 to 1000 eV where there are no laboratory sources with high intensity.

With the advent of synchrotron radiation, these problems have been resolved. The synchrotron radiation available at SSRP covers the energy region of interest with a continuous high-intensity spectral distribution. The feasibility of such radiation for X-ray lithography

has already been demonstrated at other laboratories.[†] The conclusion from this work is that X-ray lithography via synchrotron radiation can resolve lines with widths of 500 Å and should form high-quality images in the submicron region with exposure times of only a few seconds.

At SSRP, two beam ports produce radiation for nine experimental stations. The research programs have included work with physics, chemistry, biology, and medicine, are spanning the photon-energy region from 5 to 40,000 eV. Approximately 230 scientists from 30 different institutions have worked at SSRP since it began in 1974. A major expansion program began in November 1977. An experimental station for exploratory X-ray lithography was planned in this expansion.

Synchrotron radiation is, without doubt, the only available excitation source for X-ray lithography in the optimal photon-energy region of 300 to 1000 eV. The tunability of synchrotron radiation makes it possible to select photon energies that obtain the best contrast in the developed photoresist. Because the absorption coefficient varies roughly as the cube of the wavelength between absorption edges, tunability can enhance the contrast orders of magnitude.

The scattering range of secondary electrons produced in the photoresist during absorption introduces blurring in the resist and is one of the resolution-limiting factors. The range of secondaries is a very strong function of electron energy[‡] and thus excitation energy (400 Å at 1500 eV and 50 Å at 300 eV excitation energy for PMMA or other photoresist materials, for example).[*]

The high collimation of synchrotron radiation will provide greater edge definition than is achievable with a noncollimated light source. The inherent collimation of the synchrotron radiation at SSRP

[†]Spiller et al. (J. Appl. Phys., 47, 1976, p. 5450) of DESY in Germany and Fay et al. (Appl. Phys. Letts., 29, 1976, p. 370) of ACO in France.

[‡]Lindau and Spicer, J. Elec. Spect., 3, 1974, p. 409.

[*]Feder et al. J. Vac. Sci. Tech., 12, 1975, p. 1232.

is typically 0.2 to 0.3 mrad in the X-ray region. This, coupled to the high level and beam dimensions, makes the synchrotron light a very attractive source.

Discussions are under way with companies involved in VLSI (such as the Bell Laboratories) for development of the X-ray lithography line. As a result, both the resources of interest (corporations and SSRP) will probably combine to develop a practical facility that would then become available to us, and such a capability would add a significant new dimension to this work.

Overall Plan of Research

The initial emphasis will focus on making use of existing equipment and techniques. Of major importance is the development of techniques to produce useful lateral resolution for VLSI applications. This will include all available information concerning the effect of current densities on the oxides and other systems of interest.

We will obtain electron beams with the best available resolution. Varian has a commercial source with a beam diameter of approximately 2000 Å. We are working with Dr. Helmut Poppa at NASA-Ames to develop better resolution and to examine the effect of large current densities. Provision has been made for a high spatial-resolution electron gun and the necessary energy analyzer and auxiliary equipment. Before purchasing or constructing such apparatus, we anticipate testing this approach with the equipment at Varian and/or NASA-Ames to ensure that it can be utilized in this program.

The use of X-ray lithography at SSRP will be carefully explored and compared to the advanced optical equipment in operation in the IC Lab. Because the development of new X-ray lithography techniques is not planned, we will follow closely the work at SSRP and apply the technology developed there in the most optimal manner possible in this investigation.

b. The Fundamental Physics and Technology for Attaining Higher Carrier Lifetimes and Lower Defect Densities in Fabricated Silicon Devices

To attain higher carrier recombination lifetime and lower defect density in fabricated silicon devices, we are investigating the kinetics and physical mechanisms of recombination center production during processing. Emphasis is focused on those centers not caused directly by process-induced contamination but result from the intrinsic defect structure of "as grown" silicon.

There is considerable room for improved recombination lifetime. In lightly doped completely defect-free silicon, the dominant recombination mechanism would be radiative band-to-band transitions where the theoretical lifetime of silicon doped to 10^{15} cm^{-3} would be approximately 250,000 μsec [1]. Measured lifetimes as long as 2000 μsec have been observed in "as grown" float-zone silicon; however, after device processing, they are generally below 10 μsec.

The factors that control minority-carrier lifetime are some of the least understood areas of silicon-device technology. Fortunately, the operation of most devices is not greatly dependent on lifetime if it is longer than 1 μsec which corresponds to a diffusion length of 30 μm. Some devices, however, are largely dependent on the attainment of long lifetimes, such as low light-level imaging devices, solar cells, and some power devices. The refresh rate of dynamic memories is determined by generation lifetime, and many of the factors that control lifetime are probably important in achieving yields in large-scale integrated-circuit fabrication. For example, measured bulk lifetimes are often an average over a spatially inhomogeneous distribution; small areas can have a short enough lifetime to produce a defective device even when the "bulk lifetime" is sufficient [2]. The productions of point-defect recombination centers and grosser structural defects (such as stacking faults) appear interrelated through complex nucleation and precipitation mechanisms [3, 4, 5].

There is a large number of studies on lifetime and related defects in the literature [6-12], but there is no consistent overall

explanation of all the observations. It appears that in dislocation-free silicon, however, five important types of species must be considered --shallow dopants (B, P, As), transition metals (Au, Ni, Fe), oxygen, vacancies, and silicon interstitials. The complication results from the number of different interactions that occur among these species. Because the solid solubility of all these species is very low at room temperature, they tend to precipitate and form complexes while cooling down from the processing temperature. The low concentration of defects encountered (less than 10^{14} cm^{-3}) makes experimental analysis difficult.

The following observations are significant.

- Metal-vacancy clusters can form in p-n junctions resulting in soft breakdown [6].
- Transition metals migrate to highly doped regions; this is the basis of phosphorus gettering [7].
- Oxygen is present in large concentration ($\approx 10^{18}$ cm^{-3}) but is apparently inactive in its interstitial "as grown" state [8].
- Oxygen-vacancy complexes are efficient recombination centers [9].
- Oxygen complexes (believed to have four atoms) slowly form at under 600°C and are shallow donors [10].
- Oxygen precipitates to its stable phase (SiO_2) at temperatures over 700°C. The rate of precipitation is diffusion-limited [3].
- Oxygen precipitation is nucleated by a mobile species that responds to phosphorus gettering [4].
- SiO_2 precipitates can form stacking faults during oxidation that deteriorate p-n junction performance [5].
- Dopant-vacancy complexes are efficient recombination centers [11].
- Transition metals complexed with oxygen are probably less active than the metal alone. Annealing at 450°C appears to form such complexes and increases lifetime [12].

Ultimately, it would be desirable to understand the equilibrium statistics and kinetics of all of these defects so that the effect of any processing sequence could be predicted and controlled. As a first step in this direction, we will examine lifetime and other recombination parameters as a function of heat-treatment time and temperature under very clean conditions so that the effect of process-induced contamination is reduced as much as possible.

The research divides into three areas--reducing process-induced contamination, building diagnostic instruments, and studying the effects of various process parameters.

Process-Induced Contamination. Process-induced metallic contamination is a major factor in determining device lifetime and yield. This is apparent in the improved results obtained after chlorine gettering the furnace tube, even when no chlorine is present during processing [13], and in the considerable improvement observed by replacing quartz with silicon furnace tubes and boats [14]. Clearly, process-induced contamination must be reduced to the lowest possible level to achieve long lifetimes. Two sources of contamination are incomplete wafer cleaning and diffusion through the furnace tube.

Wet cleaning methods (such as boiling in acids) have limited the cleaning capability. Because of metallic contamination in the reagents, it is exceedingly difficult to obtain residual metallic surface contamination below 0.001 monolayer [15]. This relatively low contamination, if diffused uniformly through a 200 μm wafer during subsequent processing, produces a bulk concentration of 2.5×10^{13} cm^{-3} which is sufficient to limit lifetimes to below 10 μsec (however, not all surface contamination diffuses into the wafer). It is also difficult to dry the wafers without distilling out additional solution contaminates and transferring adsorbed organic films from the solution surface to the wafer surface. There is indication that plasma cleaning can resolve these problems [16]. Exposure to room air, even dust-free laminar-flow air, deteriorates clean surfaces rapidly [17,18].

It may be possible to reduce furnace contamination by using very pure silicon boats and utilizing a cold-wall system so that diffusion through the furnace tube is eliminated. Motivated by these considerations, we plan to build a low-pressure cold-wall doped oxide-deposition system that incorporates in situ plasma cleaning and has the capability of achieving diffusion temperatures of 1100°C. In this manner, wafers would receive a plasma cleaning followed by doped-oxide deposition and drive-in diffusion without exposure to laboratory air.

Diagnostic Instruments. The following measurements will be performed:

- the overall recombination rate with the open-circuit voltage-decay instrument [19]
- the depleted generation rate with MOS storage time [20]
- energy spectrum and cross sections of recombination centers with deep-level transient spectroscopy (DLTS) [21]

Only the DTLS instrumentation must be assembled; the others are available in-house. DLTS is the only known technique having sufficient sensitivity to detect the small concentration of recombination centers still present after very clean processing.

Using the level parameters as measured by DLTS, the theoretical recombination and regeneration rates will be computed and compared to the values measured through open-circuit voltage decay and MOS storage time. In this way, it will be determined if all the recombination and generation paths have been found and correctly characterized.

Effects of Processing. The recombination parameters (energy levels, cross sections, recombination, and generation rates), as measured with the above instruments, will be examined as a function of processing temperature and time under the clean conditions obtained in the cold-wall diffusion system. In this way, we hope to better understand the kinetics and physical mechanisms of recombination-center production during processing and the physical structure of these centers,

especially those that are not caused directly by process-induced contaminates but result from the intrinsic defect structure of silicon, its normal dopants, and its abundant impurities (carbon and oxygen). With this information, processes can be designed to minimize recombination-center and defect production.

Attaining a one order of magnitude increase in recombination lifetime will yield exciting improvements in low light-level image sensors and photodiodes and is crucial to our current work on thermophotovoltaic energy conversion. The ongoing program in charge-coupled devices and other large-scale integrated circuits will also benefit from positive results obtained through improved storage times and yield.

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c. Electrical and Physical Properties of Thin Thermally Grown SiO_2 Layers on Silicon

We are investigating the electrical and physical properties of thin (0 to 500 Å) SiO_2 layers thermally grown on single-crystal silicon substrates. We will study the growth kinetics, charge densities,

dielectric integrity, and enhanced oxidation effects caused by high dopant levels in the silicon substrate.

Thermal oxidation of silicon remains an essential part of integrated-circuit technologies, both bipolar and MOS, because it is used for such diverse purposes as masking against dopant diffusion, passivation of active device regions and junctions, insulating the "field regions" between active devices, and as an actual component of active MOS devices in the gate dielectric. Early in the development of silicon technology, a macroscopic model for silicon oxidation by water or dry oxygen was developed [1], based on the diffusion of the oxidizing species from the ambient through an existing oxide to react with silicon at the Si/SiO_2 interface. At different stages of the oxidation, either of two processes (diffusion of the oxidant in the oxide or reaction of the oxidant with silicon at the interface) may become the limiting step and will dominate the overall oxidation rate.

More specifically, as shown in Fig. 1, analysis based on requiring the continuity of steady-state flux of the oxidant through

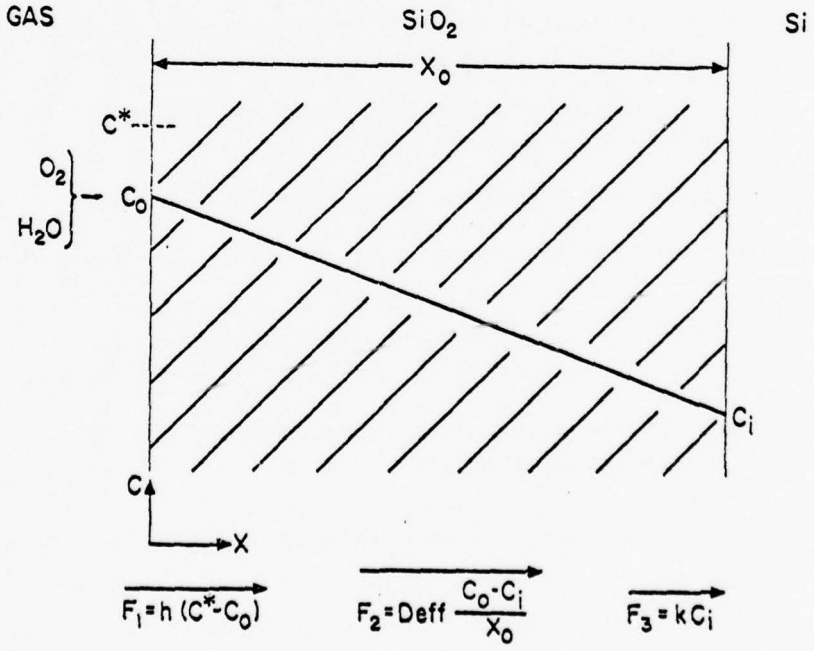

Fig. 1. BASIC PHYSICAL MODEL FOR SILICON THERMAL OXIDATION.

the ambient/oxide interface structure yields the familiar linear-parabolic growth relationship [1]:

$$\frac{x_o^2}{B} + \frac{x_o}{B/A} = t + \tau \qquad (1)$$

where

$$B = 2D_{eff}\frac{C^*}{N_1}$$

$$B/A = \frac{kh}{k + h}\frac{C^*}{N_1} \simeq k\frac{C^*}{N_1}$$

$$\tau = \frac{x_i^2}{B} + \frac{x_i}{B/A}$$

and

x_o = final oxide thickness

t = oxidation time

x_i = thickness of either an initial oxide at $t = o$ or a layer grown by an initial rapid oxidation mechanism

N_1 = number of oxidant molecules incorporated per unit volume of oxide grown

C^* = equilibrium concentration of oxidant in the oxide

D_{eff} = effective diffusion coefficient of oxidant in the oxide

h = gas-phase transport coefficient for the oxidizing species from the ambient to the outer oxide surface

k = Si/SiO_2 interface oxidation reaction-rate constant; it is generally assumed that $k \ll h$

For thin oxides and short oxidation times relative to the characteristic time $A^2/4B$, the second term on the left-hand side of Eq. (1) dominates. Linear oxide growth results, and B/A is the linear rate constant. Under these conditions, interface oxidation is reaction-rate-limited and B/A exhibits an Arrhenius temperature dependence,

$$B/A = C_o e^{-E_A/kT} \qquad (2)$$

which reflects the temperature dependence of k. The similar activation energies of approximately 2.0 eV for both dry O_2 and H_2O ambients compare favorably to the energy required to break an Si-Si bond [2], thereby suggesting that this is the rate-limiting step of the interface-reaction mechanism.

At the other extreme, for thick oxides and long oxidation times, $t \gg A^2/4B$ (and $t \gg \tau$), the first term on the left-hand side of Eq. (1) dominates, parabolic oxidation is observed, and B is the parabolic-rate constant proportional to D_{eff}; oxide growth, therefore, is diffusion-limited in the parabolic-oxidation regime. This constant also exhibits an Arrhenius temperature dependence. The activation energies of approximately 1.2 eV for dry O_2 and approximately 0.71 eV for H_2O ambients compare well to the activation energies reported for the diffusivity of oxygen and water, respectively, in fused silica, and this suggests that B reflects the temperature dependence of D_{eff} for the oxidant in the oxide [1].

Implicit in the derivation of Eq. (1) is the assumption that the oxidant species diffusing through the SiO_2 layer is molecular. Experimental evidence appears to verify this assumption because dissociation of oxygen or H_2O at the outer interface and the subsequent transport of the atomic species necessarily generate a non-first-order pressure dependence of B [3]; experimental results indicate that B increases linearly with the oxidant partial pressure from 950° to 1200°C [1,4]. This adherence to Henry's law thermodynamically implies that molecular oxygen (perhaps as a molecular ion) must be the principal diffusing species.

The macroscopic model described by Eq. (1) would also predict a first-order (linear) pressure dependence for the rate constant B/A, associated with the Si/SiO_2 interface [1]. Considerable evidence, however, indicates that, at low oxygen partial pressures and low temperatures, this dependence is not observed in B/A [5,6].

A second problem associated with the macroscopic model is its failure to predict oxidation kinetics accurately in dry O_2 for oxide thicknesses less than 200 Å [the parameters τ and x_i in Eq. (1) are often used to correct for this]. The enhanced oxidation rates observed in this initial phase are believed to be associated with space-charge layer effects in the growing oxide. If the diffusing species are at least partially molecular ions, electric field effects would be expected to play a predominant role in the growth kinetics until the oxide thickness becomes substantially larger than the extent of the space-charge region in the oxide. The extrinsic Debye length characterizes the extent of this region and, for a dry O_2 oxidation, this length is approximately 150 Å [7] which is in reasonable agreement with the experimentally observed region of enhanced growth.

Another problem with the macroscopic oxidation model is the enhanced oxidation observed over heavily doped substrate regions, and this is commonly encountered in bipolar emitter regions and MOSFET source and drain regions. Impurity doping levels often approach solid solubility.

In an idealized interpretation of Eq. (1), factors likely to influence the interface reaction rate should alter B/A, and those affecting oxidant diffusion will change B. Sufficiently high impurity levels in the substrate should modify the interface reaction. Similarly, an extremely high impurity content in the oxide may affect diffusivity of the oxidizing species. The relative magnitudes of such effects, as manifested in changes in B/A and B, should depend on a particular impurity and its behavior during oxidation.

Specifically, phosphorus, as with the other commonly used donor impurities (arsenic and antimony), diffuses more slowly in oxide than in silicon and tends to segregate at the interface in favor of higher phosphorus levels on the silicon side. As a result, a pile-up of phosphorus at the interface to levels greater than bulk concentrations in the silicon may occur during oxidation, with much lower levels in the oxide. The pile-up should also be more substantial for H_2O than for dry O_2 oxidation because of even slower diffusion relative to oxide growth

rates [8]. With phosphorus, therefore, initially high doping levels in the silicon made even greater at the interface during oxidation is expected to result in substantial changes in the interface reaction rate and, consequently, in large changes B/A. On the other hand, significantly lower phosphorus levels in the oxide may have relatively less influence on oxidant diffusion in the oxide and produce relatively smaller changes in B.

Overall, this qualitative model indicates that heavy doping levels of phosphorus (and arsenic and antimony) should have a greater influence at shorter oxidation times and lower oxidation temperatures. These effects should also be larger for H_2O than for dry O_2 oxidations. These data [9] are plotted in Fig. 2. Curves A through F correspond to increasing phosphorus doping levels (up to solid solubility). It can be observed that the enhanced oxidation effects are much more pronounced at lower temperatures and for thinner oxides. These observations qualitatively agree with the above predictions based on the macroscopic model of Deal and Grove [1]. The effects observed in Fig. 2 may be explained by mechanical (lattice strain), electrical (extrinsic conduction at oxidation temperatures resulting from high dopant concentrations--Fermi-level dependence on dopant concentration), or chemical (changes in the thermodynamics of the chemical reactions) mechanisms [9]. Redistribution and segregation are also closely connected with these enhanced oxidation phenomena.

The current understanding of silicon thermal oxidation is limited at oxide thicknesses below 500 Å for the following reasons.

- Space-charge effects that are not well modeled dominate the overall growth kinetics in dry O_2 at thicknesses up to 200 Å.
- Low partial-pressure oxidations (such as N_2/O_2 mixtures) have markedly different kinetics at low temperatures and for thin oxides (interface reaction-rate dominated) than the model represented by Eq. (1) predicts.
- Such phenomena as high substrate dopant levels that affect the interface reaction rates play their most important role in oxidation kinetics at low temperatures and for thin oxides.

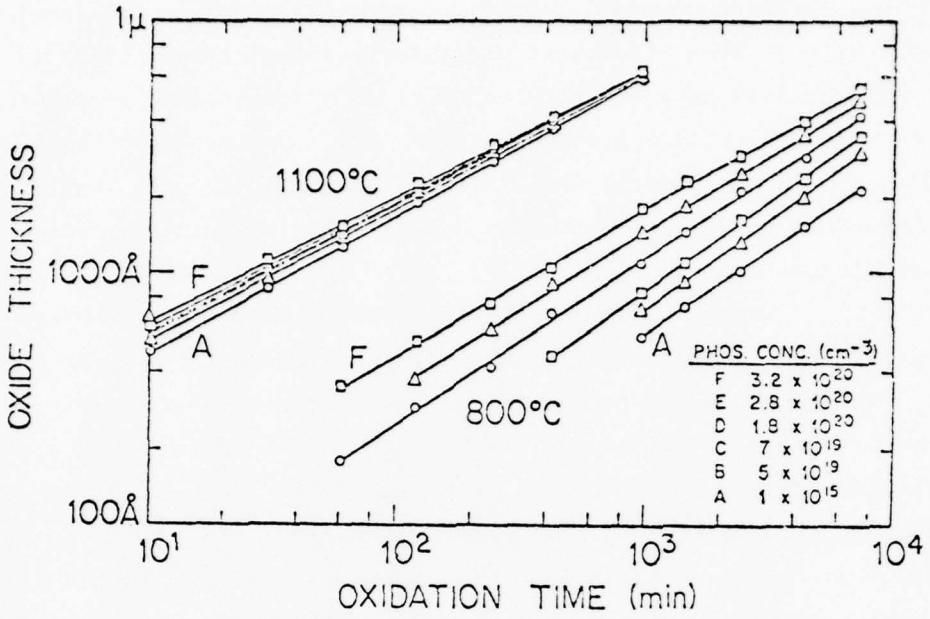

Fig. 2. SILICON-OXIDE THICKNESS VS OXIDATION TIME FOR VARYING PHOSPHORUS CONCENTRATIONS [(111) Si].

Thin-oxide kinetics is expected to be of major importance in future solid-state devices. Two significant examples are MNOS circuits that use 30 Å SiO_2 layers to achieve nonvolatile memory devices, and conventional N- and P-channel MOS integrated circuits that are tending toward thinner gate dielectrics to improve performance. Some commercially available devices make use of gate oxides ≃500 Å thick, and thinner oxides are expected in the future.

To improve our understanding of thin-oxide kinetics and properties, we propose to

gather kinetic data for thermally grown oxides in the 0 to 500 Å range

attempt to generalize the model represented by Eq. (1) to include an accurate prediction of these kinetics under all important processing conditions

investigate the dielectric integreity of these thin oxides if they are to be used as gate dielectrics in future MOS devices

- analyze the fixed surface state density (Q_{ss}) and interface state density (N_{st}) in these thin oxides because the parameters are also of significant importance if these oxides are to be useful in MOS devices

This program is designed to complement a current Defense Advanced Projects Agency sponsored process-modeling program (Contract No. DAAB07-75-C-1344) under which advanced process models and computer-simulation programs for oxidation, diffusion, ion implantation, and epitaxy are being developed.

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d. Modeling of the Small-Geometry Devices for VLSI

We are attempting to determine performance limits as device geometries are reduced and, as a result, surface conduction, oxide properties, and process-induced defects must be studied within the context of fine-geometry structures. The modeling and characterization of these effects will become essential data for the next generation of electronics. Because many physical limits are being approached simultaneously at submicron dimensions, it is no longer reasonable to "scale" dimensions [1,2] without a more thorough analytical understanding. This section describes specific research activities designed to generate the test structures and analytical models necessary to explore the physical and electrical effects in submicron silicon devices.

Figure 3 is a cross section of a small-geometry MOS transistor. Device dimensions L, δL, θ, and t_{ox} are identified, and the circled numbers indicate regions impacted by the following studies.

(1): surface-conduction studies relating to transport phenomena between source and drain

(2): oxide studies pertaining to the effects under the gate and near the source and drain

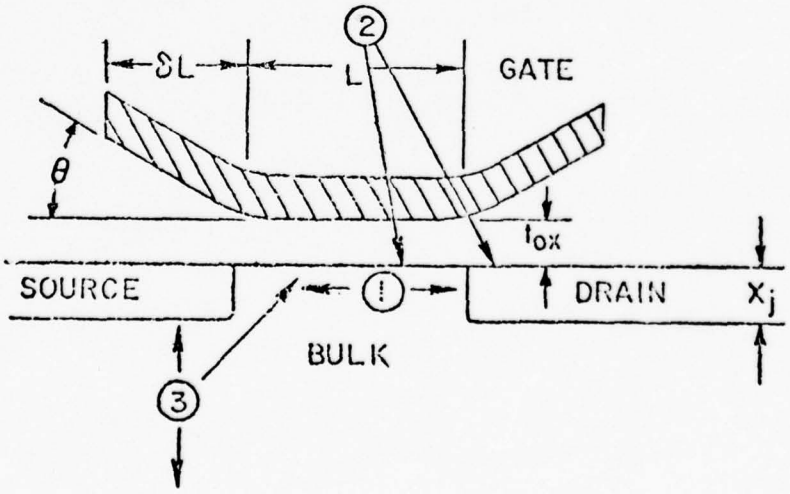

Fig. 3. SMALL-GEOMETRY MOS TRANSISTOR.

③: process-induced defect studies that apply everywhere in the bulk, source, drain, and surface

To characterize the effects of each set of phenomena on the device level, however, area dependencies must be included. For example, oxide breakdown depends strongly on drain fields and, therefore, on voltages and geometry; similarly, leakage, punchthrough, and junction breakdown depend on junction profiles, defects, and the electrode configuration. Surface conductance depends on surface roughness, interface states, and other conditions that cause variations in the surface potential. Although Fig. 3 emphasizes the MOSFET transistor, surface-conduction limits are also apparent for CCDs [2]. This research will investigate surface conduction, oxide, and defect limits for MOS and CCD devices with minimum dimensions of $<1\mu$.

The following dimensional limits are expected to control device parameters as physical dimensions become smaller.

- Thin oxides have uncertainties because of the fabrication limits of initial oxide thickness τ_o and tunnel length τ_e for electrons.
- Debye length L_D is a limit on depletion-layer effects and subthreshold conduction parameters [3,4].
- Defects introduce limits that will be defined by two parameters.
- Point defects alter bulk lifetime τ.
- Mask-edge and strain-induced problems are characterized by L_α.
- Fluctuations in surface dimensions and interface charge are characterized by a dimensional δ_i.

As the physical dimensions approach these sizes, device performance can be altered substantially. We will explore each of these dimensional limits within the context of measured and simulated carrier transport, and the results of this work will determine how the physical limits couple and ultimately control the performance of small-geometry devices.

Test Structures

To define test structures for submicron technologies, several observations are essential. First, one-dimensional approximations are invaluable for the limiting case. Second, edge effects can be used as boundary conditions for simulations and measurements on fine-geometry devices. Figure 4 illustrates each of these points for specific MOS device effects. Figures 4a and 4b represent one-dimensional structures--conventional large MOS and MOSFET devices; surface conduction, oxide charge, and bulk-lifetime effects are best characterized using these well-known tools. Figures 4c and 4d

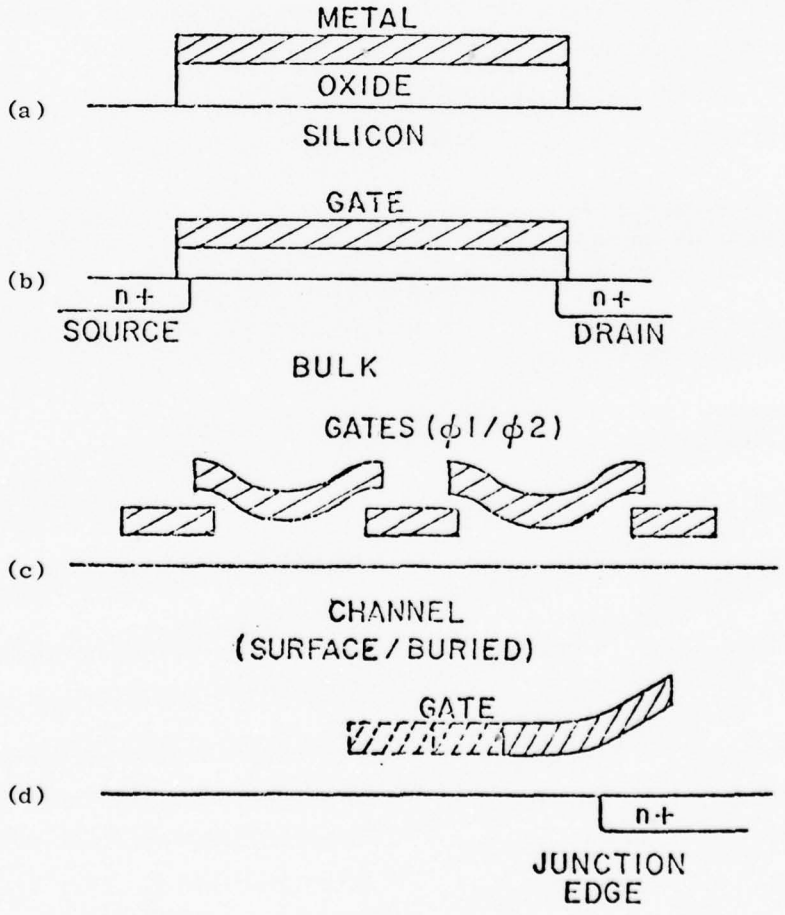

Fig. 4. TEST STRUCTURES FOR SUBMICRON TECHNOLOGIES.

represent small-geometry structures essential for the analysis of edge effects. In particular, the CCD (Fig. 4c) is a primary tool with which to consider surface and buried-channel transport limits, independent of source/drain terminations. Asymmetries in surface transport with bias conditions for both dc and transient analyses are considered, and the parametric effects associated with gate length, oxide thickness, and charge scaling (L, t_{ox}, and δ_i) will be determined. Figure 4d is a gated-diode configuration for fine-geometry studies, focusing on edge effects. Process-induced defects can be examined parametrically with x_j, t_{ox} and L variations, and the effects associated with δL, θ, and edge profiles in the n^+ region can be explored. The following discussion will expand on the experiments to be pursued based on such structures as those illustrated in Figs. 4c and 4d.

None of these test structures provides any new innovations; however, the careful exploration of device transport and edge effects as an adjunct to the fundamental studies is essential. A better understanding will be gained from investigation of the effects of device parameters L, δL, θ, and x_j and physical parameters t_{ox}, τ_e, L_D, L_α, τ, and δ_i on electrical transport. In the CCD, the statistical effects associated with L, t_{ox}, gap spacing, and oxide charge must be characterized. The first step is to analyze the CCD carefully as each of these parameters is altered systematically so as to define limiting cases where physical parameters rather than design parameters control transport. Testing for edge effects includes a variety of experiments. The dependence of lifetime degradation at mask edges caused by strain and implantation knock-on is one important set of experiments. A second is the interaction of the n^+ doping and lateral diffusion with local lifetime, oxide thickness (including θ dependence), and oxide charges.

MOSFET Device Studies

The data obtained to characterize the effects of key parameters can be used in limiting-case experiments for comparison to simulation. A two-dimensional device-simulation program is available for MOSFET analysis. Simulation of the test structures in Figs. 4c and

4d will serve initially to calibrate the program and facilitate understanding of parameter sensitivities. Next, small-geometry MOSFETs will be fabricated, and two-dimensional effects that cannot be characterized by fabrication perturbations will be simulated. Based on the earlier studies of edge effects and the understanding of transport limits, the observed device limits will be determined by simulation. Two examples illustrate this approach. First, edge effects and lifetime degradation will be analyzed because they substantially alter subthreshold conduction and avalanching, and simulation can most easily characterize these effects in two-dimensions; the coupling of measurements and simulation will define the parametric limits of these transport effects. Second, the limits imposed by oxidation and surface conduction will be investigated for both short-channel MOSFET and CCD structures. The following cases will be simulated and studied experimentally:

- surface-conduction limits based on δ_i, τ_o, and τ_e
- edge transport and charge-storage limits related to L, δL, and θ

Defects and edge-induced effects in carrier transport can become very important in small-geometry MOS devices. As diffused regions become smaller, the dominance of space charge and edge effects becomes apparent. The contribution of τ must first be characterized, and then the separation of edge-induced lifetime effects and interface-controlled properties must be identified. It has been reported [5] that subthreshold conduction properties of small-geometry devices can be substantially altered by channel length and source doping (diffusion vs ion implantation). Similarly, minority-carrier effects associated with drain-region punchthrough and avalanching must be studied.

The two sets of problems associated with surface conduction have been identified. First, the oxide-limiting effects are characterized by δ_i, τ_o and τ_e, and the granularity of surfaces and oxides are most apparent as t_{ox} approaches δ_i and τ_o. The results of oxide charge storage become more severe as t_{ox} approaches τ_e. These problems will be pursued, using both large- and small-geometry

structures, and the effects and model coefficients are determined experimentally in large-geometry devices (Figs. 4a and 4b). Based on simulation and measurements for submicron devices, the limits caused by δ_i, τ_o, and τ_e will be evaluated. Second, edge transport and charge-storage limits as determined by L, δ_i, and θ will be analyzed because they impact both FETs and CCDs. Fringing field effects can be expected to be even more important at submicron dimensions. To study these effects, large-geometry devices are ineffective and, therefore, CCDs and short-channel FETs are essential. By controlling lateral impurity diffusion and oxide growth over the source and drain regions [6], structures with controlled ΔL and θ can be formed. Similar CCD conditions can be created for two-level polysilicon structures. The results of these studies will yield significant geometric constraints on edge transport limited by L, δL, and θ.

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e. Submicrowatt Bipolar Integrated-Circuit Design

The full capabilities of bipolar integrated circuits have as yet to be realized. Although it is now possible to produce bipolar

IC transistors with betas greater than 50 for both NPNs and PNPs at current levels of 10 nA and less, the integrated-circuit design has not advanced with the process improvements and, as a result, few ICs utilize the full current range of bipolar transistors. Increased VLSI circuit complexity, such as I^2L processing of analog signals, will require this technology to maintain a reasonable power level for low-power systems. To meet this new emphasis, we plan to develop specific designs in the following areas:

- fully integrated ultra-low power regulated bias supplies
- low-current high-gain wide-bandwidth stages for input interfaces
- less than 1 V circuit design to realize the full potential of bipolar silicon transistors that require only 0.35 V V_{BE} and less than 0.10 V V_{CE} in the 1 to 10 nA range

The need for low-power integrated circuits is increasing at a remarkable rate; applications include medical instrumentation (such as pacemakers and implanted monitoring equipment), personal communication systems (such as pocket pagers), military field instruments, and consumer electronics (such as smoke detectors and camera-control systems). Much of this activity relies on MOS technologies because of the relatively low performance of pre-1977 bipolar devices in the submicroamp range. The introduction of I^2L and increased interests in the basic limits of bipolar devices have resulted in NPNs and PNPs with flat betas down to 1 nA. No comparable quantum jump in the integrated-circuit design has yet been achieved to utilize fully this new bipolar-process capability; we plan to explore this design area. Significant limits anticipated include substrate leakage on the order of 1 pA, parasitic capacitances that, without careful design, may result in >5 msec time constants in the systems, and extremely high resistances (>100 MΩ/IC) if conventional bias and gain modules are used. The rewards are in realizing

- sub-microwatt bipolar ICs that operate at a supply of less than 1 V
- bipolar ICs that compare favorably to MOS devices with respect to input bias
- techniques that can be utilized in virtually all linear low-power designs

This work is essential to realize fully integrated electronic systems that do not require a large number of costly discrete elements. Reliability is increased, and parasitic leakages decreases as the degree of integration is raised from the circuit to the system levels.

The basic process used today in standard linear bipolar integrated circuits originated in 1965 to 1968 [1]. As current is decreased, this process has a beta rolloff of roughly 50%/decade below 30 μA and is used in the most widely distributed linear ICs, including the 301, 318, and 741 operational amplifiers, the 733 wideband amplifier, the 796 wideband mixer, and the 370 AGC amplifier. Minor perturbations in this process, such as in the super-beta transistor, have been introduced to reduce input bias [2]. The most notable IC in the group is the 308 operational amplifier. A few specialty processing houses have developed high-performance versions of all of these ICs through special processing, but the majority of linear ICs is from the 1969 vintage and most of the special processing techniques have been closely guarded as trade secrets.

To fill the need for high performance with low bias currents, RCA developed the BIMOS process in 1974 [3] and, for high enough voltages (>2.5 V), the CA 3130 and CA 3140 op amps achieve extraordinary performance. This process can produce a number of useful circuits at extremely low currents. A 100 nA op amp with a gain of 88 dB and a gain-bandwidth product of 7 kHz has been built [4]; its current is programmed externally, and total drains of less than 10 nA have been realized at the expense of the gain-bandwidth product. The performance of this merged bipolar and MOS process is limited because of early bipolar-transistor rolloff. It should be noted that, at current levels below 1 μA, the MOS devices are exponential rather than square law and that

their transconductance only approaches the bipolar g_m of I/26 mV; typical by, in this region, g_m = I/40 mV.

An alternative developed by Texas Instruments and National Semiconductors is a bipolar and junction FET (BIFET) process which is primarily a variation on the 1968 version with the addition of an ion-implanted JFET [5]. It provides a low input bias, low noise, and wide dynamic range but is not well suited for ultralow current applications because of beta rolloff in the NPNs.

Within the past year, Werner [6] has published a bipolar process that achieves flat betas (+0, -10%) down to 1 nA, and work in the Stanford Integrated-Circuits Laboratory has resulted in similar performance for both upward and downward NPNs to 5 nA with only minor perturbations in the present processes [7]. Additional activity at Stanford will include the creation of a table of processing trade-offs to be used to achieve ultralow current bipolar devices. Process perturbations may include the effects of argon annealing, nitride passivation, and low concentration emitters on beta rolloff [8].

National Semiconductors has also developed an ultralow current bipolar process for a camera-control IC. It utilizes the low-current features not so much to save power but to realize amplification and signal processing of low currents generated from integrated photodiodes (~4 nA). The power drain of this chip is in excess of 1 mW when operational.

In many situations, power must be continuously maintained and power levels below 1 μW must be realized; pacemakers, volatile battery-powered bipolar memories, and continuous monitors (such as implanted medical instrumentation or remote field sensors) are a few examples. To achieve this goal, current supplies below 100 nA must be developed and low-current gain stages and low-voltage design should be explored.

The following areas of principal concern will be addressed in the research:

- high-efficiency small bias circuits
- input stages with wide bandwidth, low noise, and high transconductance
- ultralow (<1 V) circuit design

The bias circuit is required to generate a controlled current (or voltage) for submicroamp ICs. Conventionally, either an off-chip resistor or a greater than 10:1 step-down current repeater has been used in these applications; the resistor is an additional element and is often larger than the IC, and the step-down circuit is usually less than 10 percent efficient--a significant waste of power in systems intended to consume the minimum possible power. The work on bias generation will involve theoretical, computer, and circuit realizations of various self-starting circuits. Low currents may be generated through feedback and a step-down mirror with only a 2:1 ratio so that it would be necessary for the integrated resistor in the mirror only to support 17 mV. As a result, a 1.7 MΩ resistors, which can be integrated, could develop a regulated 10 nA current.

The work in the input-stage design is of interest because of the large number of systems requiring low bias current such as op amps, charge-sensitive devices such as sample-and-hold amplifiers, or even ion-sensitive sensors such as smoke detectors and pH electrodes. Conventional differential stages operating with a 1 to 10 nA collector will be analyzed with respect to input offsets, frequency response, and noise. Compound stages and frequency enhancement may also be considered. Again, this work will focus on all three areas of theoretical, computer-aided, and integrated design.

The last research area is a truly unique extension of operating the bipolar device at submicroamp current levels. A V_{BE} of 0.36 V and a V_{CE} of less than 100 mV are possible at 1 nA collector currents; thus, multiple transistors can be stacked and still operate with less than a 1 V supply. This extends the operating range of batteries and may introduce new functional modules not generally available in low-voltage operation.

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G. The Transport Properties of $Al_xGa_{1-x}As$ Single Crystals

Principal Investigator: G. L. Pearson

1. Objectives

This research is a systematic study of the transport properties of free carriers in the ternary semiconductor system. The electronic parameters are free carrier mobility, resistivity, minority-carrier diffusion length, impurity activation energy, and trap-energy levels. The distribution coefficients of selected doping impurities as a function of composition x are significant growth parameters. The results obtained should prove useful in the design of photoluminescent devices, injection lasers, solar cells, infrared detectors, and bulk-effect microwave devices.

2. Current Status of Work

Single-crystal layers of $Al_xGa_{1-x}As$ have been grown throughout the composition range of $0.0 < x < 1.0$ on GaAs substrates, using liquid-phase epitaxial techniques. The aluminum-distribution coefficient and growth rate have been determined for LPE growth in the temperature interval of 800° to 785°C. The dopant impurities were Ge for p-type layers and Sn for n-type layers.

Hall measurements have been performed on several sets of $Al_xGa_{1-x}As$:Ge and $Al_xGa_{1-x}As$:Sn LPE crystals grown through semi-insulating GaAs:Cr substrates. The carrier-concentration variation with temperature was used to obtain the thermal-ionization energies of the Ge acceptor and Sn donor in $Al_xGa_{1-x}As$ as a function of composition x. The carrier concentration at 300 K and the known doping level in the $Al_xGa_{1-x}As$ melts determined the Ge and Sn distribution coefficients in crystals grown in the temperature interval of 800° to 785°C. Additional Hall measurements are being made on the Al-rich compositions of $Al_xGa_{1-x}As$:Sn to achieve more reproducible results.

A series of (p)$Al_xGa_{1-x}As$:Ge layers grown on (n^+)GaAs:Te substrates were investigated. Diodes cleaved from the wafers were

characterized by capacitance-voltage and current-voltage measurements so as to analyze the properties of the (p)$Al_xGa_{1-x}As$-(n)GaAs heterojunction as the Al composition is varied. The electron-diffusion lengths in the (p)$Al_xGa_{1-x}As$ layers were determined from the decay of the short-circuit current which was induced as the electron beam of an SEM was scanned across the p-n junction. Additional studies are planned for the growth and characterization of (n)$Al_xGa_{1-x}As$-(p)GaAs heterojunctions.

We plan to continue experimental measurements of the electrical properties of $Al_xGa_{1-x}As$ and to develop a model for the compositional and temperature dependence of the electronic transport in $Al_xGa_{1-x}As$.

3. Achievements

The $Al_xGa_{1-x}As$ system has proved to be very attractive for the fabrication of optoelectronic devices such as diode lasers, LEDs, and highly efficient solar cells because the nearly exact lattice match between GaAs and AlAs enables the growth of heterostructures with nearly ideal interfaces and band-gap energies ranging from 1.43 to 2.16 eV. Although the preparation and optical properties of $Al_xGa_{1-x}As$ and heterostructure devices have been studied extensively, our systematic investigation of the electronic properties should be very useful in the design of such electronic devices as AlGaAs field-effect transistors.

The minority-carrier diffusion length is one of the principal properties that governs the performance of semiconductor devices. Although several studies have been made using GaAs, very little data are available concerning the $Al_xGa_{1-x}As$ system. We have measured the electron diffusion lengths in (p)$Al_xGa_{1-x}As$ from the decay of induced current as the electron beam of an SEM is scanned across the edge of a p-n junction. It was observed that the electron diffusion length in GaAs is 7 μm, decreases to 2 μm for $Al_{0.4}Ga_{0.6}As$:Ge, and remains at ≈1 μm for $x > 0.5$. Additional studies are planned to measure the hole-diffusion length in (n)$Al_xGa_{1-x}As$:Sn.

H. Application of Maximum-Entropy Method to Transhorizon Propagation Measurements

Principal Investigator: A. T. Waterman, Jr.

1. Objective

The initial purpose of this research is to work with data obtained previously from S-band transhorizon experiments and to analyze these data by maximum-entropy techniques. Because these techniques are capable of greater resolution and accuracy than conventional Fourier methods, it is conceivable that features of the data previously unobserved may be revealed.

2. Current Status of Work

This work has just begun. Its progress, thus far, is the result of the fortunate circumstance of our having a visiting scientist from the Norwegian Defense Research Establishment who became interested in the concept and worked on it at no cost to the project. He has received and analyzed large quantities of data obtained at Stanford by N. Cianos, in which the 12-element receiving antenna array was oriented vertically so that the beams were narrow in elevation and wide in azimuth (unlike the present orientation).

More of the past data will be studied in this manner. The current data obtained with the antenna array oriented horizontally will be analyzed by maximum entropy wherein the following two approaches will be tried:

- Fourier decomposing the doppler spectrum and applying maximum entropy to each doppler band
- forming Fourier beams and applying maximum entropy to the doppler spectrum

A true two-dimensional maximum-entropy approach may be attempted if the computational difficulties can be reduced to manageable proportions. If this can be accomplished satisfactorily, it can be applied not only to the two dimensions of angle and doppler, but also to a

two-dimensional array where the 12 elements will be rearranged into a 3×4 element array or into two linear six-element arrays--one vertical and one horizontal. Perhaps even more elements can be added to form a larger structure. The precise route to follow will depend on the results achieved at intermediate stages.

3. Achievements

The most clearcut result evident at this stage is the distinct identification of scattering from turbulent layers. The height of the layer as determined by elevation angle and the height as measured in refractometer flights are in very close agreement. In the maximum-entropy analysis, the location of the layer is unambiguous; in the Fourier analysis the layer is often lost in the sidelobe structure. This appears to be a positive result that would not be possible without the maximum-entropy technique.

I. Tropospheric Radio Propagation

Principal Investigator: A. T. Waterman, Jr.

1. Objective

The objective of this research is to investigate atmospheric parameters and phenomena in the lower troposphere based on radio propagation in the S-band. The goals are to

- measure wind velocity in the common volume of a trans-horizon troposcatter propagation path by means of doppler techniques
- probe the structure of winds and turbulence in the lower troposphere under various conditions of atmospheric stability and instability.

The plan is to receive simultaneously 3 GHz CW signals, from a transmitter located 100 miles away (beyond line-of-sight), on each of two narrow beams aimed on either side of the great-circle bearing toward the transmitter by small amounts (1° or less). If a wind component is transverse to the path in the region of the common volume, it is anticipated that the signal received on one beam will be doppler shifted to higher frequencies and that the signal on the other will be shifted to lower frequencies. The magnitude of the doppler difference should be proportional to transverse-wind velocity. The two beams will be formed during data reduction because the receiving antenna is a sampling array that measures and stores on digital tape the amplitudes and phases of the signal as received on 12 individual antennas. To obtain high azimuthal resolution, the antennas are arranged in a horizontal linear array. This research relates to the preceding program because the high resolution achievable with maximum-entropy techniques is applied to the propagation data received on the array.

2. Current Status of Work

During a 48-hour period from 20 to 22 April 1978, the equipment was operated as planned; the transmitter was positioned at Jackson,

California, and the receiver and array were located at the field site on the Stanford campus. Data were obtained during a continuous 10 min period each hour. Calibration checks were run before and after each hourly data sample. Arrangements were made with the Meteorology Department of San Jose State University to take conventional winds-aloft measurements by tracking pilot balloons with a theodolite. These measurements were made from a site near Livermore, directly under the common volume of the transhorizon path, and nearly simultaneously with the periods of radio-data gathering. The weather was good throughout the run although the wind was calmer than may have been desired for measuring wind from the radio data. All equipment operated satisfactorily.

Data obtained during the run are being analyzed, and several consistency checks have been made (such as apparent antenna-beam bearing vs surveyed bearing and zero-doppler offset vs relative oscillator drift). For the wind analysis, the following procedure (one among several to be used) has been initiated. Starting from the amplitude and phase data as received on each antenna element (sampled 40 times/sec), a 45-sec interval (1800 data points) was Fourier decomposed into doppler frequency components. For every component, a beam pointing in a given direction was synthesized and, for each direction, the response was then plotted as a function of doppler offset.

3. Achievements

Although the data analysis is in an early stage, preliminary results are illustrated in Fig. 5 where doppler spectra for four pairs of symmetrical off-path antenna pointings plus two on path are presented. The doppler-offset scale runs from -5 to +5 Hz. The ordinate (signal level) is logarithmic, 2 dB per fine division. The strong signal appearing near the center of the spectrum (zero doppler) at all angles corresponds to a layer reflection or knife-edge diffraction. There is also a doppler signal whose frequency offset increases (in the negative frequency direction) as the antenna beam is aimed farther to the left of the great-circle bearing; when the beams are aimed to the right, there is a hint of the corresponding positive doppler offset. These offsets are

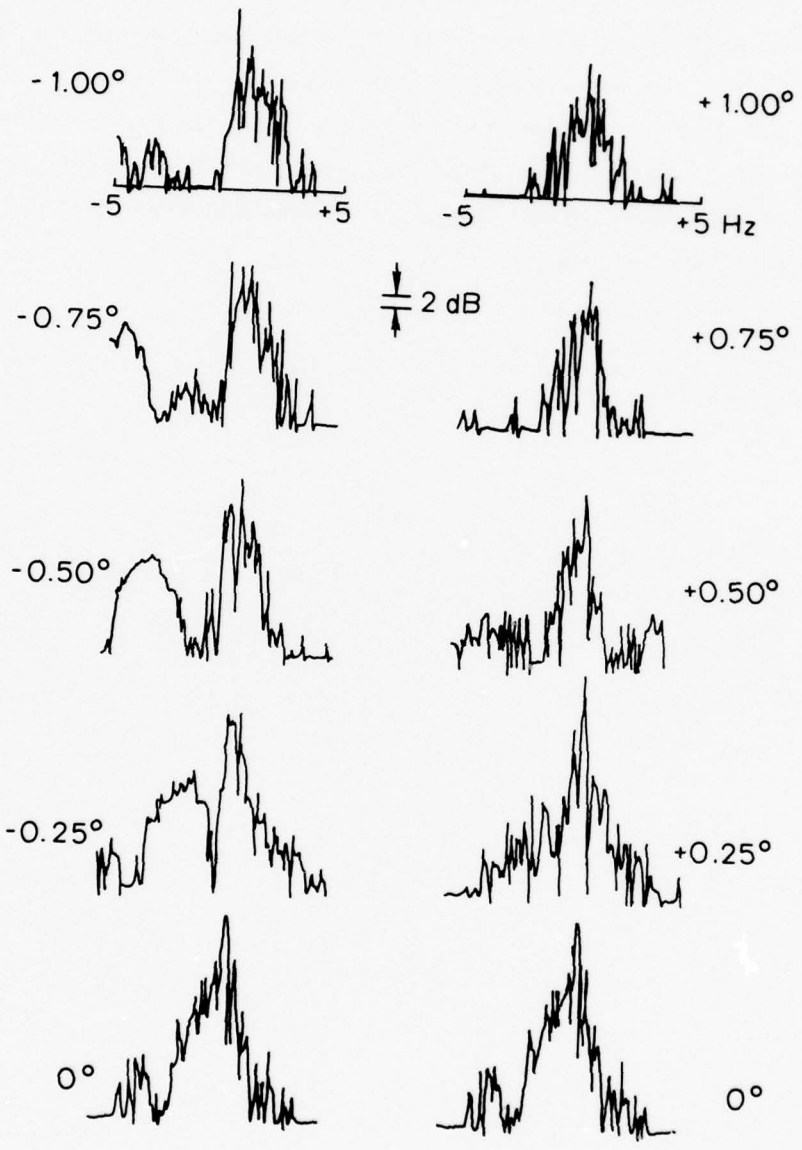

Fig. 5. RESPONSE VS DOPPLER FREQUENCY FOR DIFFERENT AZIMUTHS. Doppler spectra: 1800 scans.

analogous to a wind moving from right to left across the path as viewed from the receiver. Insufficient data have been analyzed to determine this motion precisely, but the wind is of the right magnitude to be consistent with the meteorological measurements.

We plan a detailed analysis of all the data acquired during the April run. The doppler offset on individual beams will also be compared to the width of the amplitude fading spectrum when receiving simultaneously on two beams.

J. Generation of Intense Microwave Radiation

Principal Investigator: F. Crawford

1. Objectives

The aim of this project is to design and construct a high-power magnetron capable of producing ~1 GW ~1 μsec (~1 kJ energy) pulses at ≈3 GHz. The tube components and power supplies have been designed and are now being manufactured.

2. Current Status of Work

Work is continuing on scaling up in power the high-power long-anode magnetron tube of Boot et al. [1] to the relativistic electron-energy range. The anode block has been designed, a prototype constructed, and the normal modes identified by standard cold-testing techniques [2]. To arrive at a satisfactory design for the coupling-out structure, a variety of magnetically coupled plates is being tested in a full-scale mock-up of the tube. This procedure will result in the design of a structure that will transform the anode-block π mode into an E_{01} cylindrical waveguide mode, provide selectivity against coupling out unwanted modes, and act as a weak strap to ensure that the block is oscillating in the π mode.

The order for the specially constructed high-voltage pulse generator and associated power supply was placed after detailed considerations of bids from three manufacturers. Its cost has been covered primarily by a grant from the Physics Division of the NSF and a matching grant from the Stanford University School of Engineering. The pulser system has been manufactured, and acceptance testing is under way. Similarly, the design characteristics of the oxide cathode have been specified after consultations with an outside vendor who has manufactured the individual parts and is now completing the indirectly-heated cathode assembly.

Several other groups in this country (NRL, MIT, LLL) and in the Soviet Union are doing related work on relativistic microwave oscillators, and we are in contact with those in this country.

The tube will be assembled and tested during the new funding period, with the aim of locating the operating parameters for stable and reliable oxcillation.

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3. Achievements

The specially designed high-voltage pulser (500 kV and 15 kJ of stored dc energy) has been delivered and is now being tested for acceptance. The magnetron oxide-cathode components have been manufactured, and the cathode assembly will be completed shortly. A full-scale mock-up of the tube assembly has been used to verify the design calculations for the anode block and to define the geometry of the coupling-out structure.

II. OUTSIDE PUBLICATIONS

INFORMATION SYSTEMS

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